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ITG-3701
Register Map and Description
Revision 1.0

CONTENTS

1 Revision History

Revision Date	Revision	Description
06/09/2014	1.0	Initial Release

2 Purpose and Scope

This document is a preliminary register map description document, providing register information for gyroscope devices in the table below.

Specifications are based upon design analysis and simulation results only. Specifications are subject to change without notice. Final specifications will be updated based upon characterization of production silicon.

Following device is covered in this document:

Device Part Number	# of Axis	Package size (mm)
ITG-3701	3, XYZ	3.0x3.0x0.75

3 Register Map

The register map for the ITG-3701 is listed below.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04	04	XG_OFFS_TC_H	R/W	-	-	-	-	-	-	XG_OFFS_TC_H [9]	XG_OFFS_TC_H [8]
05	05	XG_OFFS_TC_L	R/W	XG_OFFS_TC_L [7:0]							
07	07	YG_OFFS_TC_H	R/W	-	-	-	-	-	-	YG_OFFS_TC_H [9]	YG_OFFS_TC_H [8]
08	08	YG_OFFS_TC_L	R/W	YG_OFFS_TC_L [7:0]							
0A	10	ZG_OFFS_TC_H	R/W	-	-	-	-	-	-	ZG_OFFS_TC_H [9]	ZG_OFFS_TC_H [8]
0B	11	ZG_OFFS_TC_L	R/W	ZG_OFFS_TC_L [7:0]							
13	19	XG_OFFS_USRH	R/W	X_OFFS_USR[15:8]							
14	20	XG_OFFS_USRL	R/W	X_OFFS_USR[7:0]							
15	21	YG_OFFS_USRH	R/W	Y_OFFS_USR[15:8]							
16	22	YG_OFFS_USRL	R/W	Y_OFFS_USR[7:0]							
17	23	ZG_OFFS_USRH	R/W	Z_OFFS_USR[15:8]							
18	24	G_OFFS_USRL	R/W	Z_OFFS_USR[7:0]							
19	25	SMPLRT_DIV	R/W	SMPLRT_DIV[7:0]							
1A	26	CONFIG	R/W	-	FIFO _MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
1B	27	GYRO_CONFIG	R/W	XG_ST	YG_ST	ZG_ST	FS_SEL [1:0]		-	FCHOICE_B[1:0]	
23	35	FIFO_EN	R/W	TEMP _FIFO_EN	XG _FIFO_EN	YG _FIFO_EN	ZG _FIFO_EN	-	-	-	-
37	55	INT_PIN_CFG	R/W	INT_LEVEL	INT_OPEN	LATCH _INT_EN	INT_RD _CLEAR	FSYNC_ INT_LEVEL	FSYNC _INT _MODE_EN	-	-
38	56	INT_ENABLE	R/W	-	-	-	FIFO _OFLOW _EN	FSYNC_INT _EN	-	-	DATA _RDY_EN
3A	58	INT_STATUS	R	-	-	-	FIFO _OFLOW _INT	FSYNC_INT	-	-	DATA _RDY_INT
41	65	TEMP_OUT_H	R	TEMP_OUT[15:8]							
42	66	TEMP_OUT_L	R	TEMP_OUT[7:0]							
43	67	GYRO_XOUT_H	R	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT_L	R	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT_H	R	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT_L	R	GYRO_YOUT[7:0]							
47	71	GYRO_ZOUT_H	R	GYRO_ZOUT[15:8]							
48	72	GYRO_ZOUT_L	R	GYRO_ZOUT[7:0]							
6A	106	USER_CTRL	R/W	-	FIFO_EN	-	I2C_IF _DIS	-	FIFO _RESET	-	SIG_COND _RESET
6B	107	PWR_MGMT_1	R/W	DEVICE _RESET	SLEEP	-	-	TEMP_DIS	CLKSEL[2:0]		
6C	108	PWR_MGMT_2	R/W	-		-	-	-	STBY_XG	STBY_YG	STBY_ZG
72	114	FIFO_COUNTH	R/W	-	-	-	-	-	-	FIFO_COUNT[9:8]	

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
73	115	FIFO_COUNTL	R/W	FIFO_COUNT[7:0]							
74	116	FIFO_R_W	R/W	FIFO_DATA[7:0]							
75	117	WHO_AM_I	R	-	WHO_AM_I[6:1]						-

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables that follow, register names are in capital letters, while register values are in capital letters and italicized. For example, the GYRO_XOUT_H register (Register 67) contains the 8 most significant bits, *GYRO_XOUT*[15:8], of the 16-bit X-Axis gyroscope measurement, *GYRO_XOUT*.

The reset value is 0x00 for all registers except for the WHO_AM_I register (Register 117), which resets to 0x68.

4 Register Descriptions

This section describes the function and contents of each register.

Note: The device will come up in full power mode upon power-up. (i.e. not sleep mode)

4.1 Registers 04-05, 07-08, 10-11- Gyroscope offset Temperature Compensation (TC)

XG_OFFS_TC_H, XG_OFFS_TC_L, YG_OFFS_TC_H, YG_OFFS_TC_L, ZG_OFFS_TC_H, and ZG_OFFS_TC_L

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04	04							XG_OFFS_TC_H [9]	XG_OFFS_TC_H [8]
05	05	XG_OFFS_TC_L [7:0]							
07	07							YG_OFFS_TC_H [9]	YG_OFFS_TC_H [8]
08	08	YG_OFFS_TC_L [7:0]							
0A	10							ZG_OFFS_TC_H [9]	ZG_OFFS_TC_H [8]
0B	11	ZG_OFFS_TC_L [7:0]							

Description:

The temperature compensation (TC) registers are used to reduce gyro offset variation due to temperature change. The TC feature is always enabled. However the compensation only happens when a non-zero TC coefficient is programed during factory trim which gets loaded into these registers at power up or after a *DEVICE_RESET*. If these registers contain a value of zero, temperature compensation has no effect on the offset of the chip. The TC registers are 10-bit signed values in 2's complement format with a resolution of 2.52 mdps/C steps.

If these registers contain a non-zero value after power up, the user may write zeros to them to see the offset values without TC with temperature variation. Note that doing so may result in offset values that exceed data sheet "Initial ZRO Tolerance". The TC coefficients maybe restored by the user with a power up or a *DEVICE_RESET*.

Parameters:

XG_OFFS_TC_H/L: 10-bit offset of X gyroscope (2's complement)

YG_OFFS_TC_H/L: 10-bit offset of Y gyroscope (2's complement)

ZG_OFFS_TC_H/L: 10-bit offset of Z gyroscope (2's complement)

4.2 Registers 19 to 24 – Gyroscope offset adjustment

XG_OFFS_USRH, XG_OFFS_USRL, YG_OFFS_USRH, YG_OFFS_USRL, ZG_OFFS_USRH, and ZG_OFFS_USRL

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13	19	X_OFFS_USR[15:8]							
14	20	X_OFFS_USR[7:0]							
15	21	Y_OFFS_USR[15:8]							
16	22	Y_OFFS_USR[7:0]							
17	23	Z_OFFS_USR[15:8]							
18	24	Z_OFFS_USR[7:0]							

Description:

These registers are used to remove DC bias from the sensor outputs. The values in these registers are subtracted from the gyroscope sensor values before going into the sensor registers (see registers 67 to 72).

Parameters:

XG_OFFS_USR_H/L: 16-bit offset of X gyroscope (2's complement)

YG_OFFS_USR_H/L: 16-bit offset of Y gyroscope (2's complement)

ZG_OFFS_USR_H/L: 16-bit offset of Z gyroscope (2's complement)

4.3 Register 25 – Sample Rate Divider SMPRT_DIV

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19	25	SMPLRT_DIV[7:0]							

Description:

This register specifies the divider from the gyroscope output rate that can be used to generate a reduced Sample Rate. Please note that this register is only effective when *FCHOICE_B*[1:0] = 2'b00 (Register 27) and *DLPF_CFG* = 1, 2, 3, 4, 5, or 6 (Register 26).

When *FCOICE_B*[1:0] = 2'b00 but *DLPF_CFG* = 0 or 7, the Sample Rate is fixed at 8kHz and the divider in this register does not apply. When *FCHOICE_B*[1:0] = 2'b01, 2'b10, or 2'b11, the Sample Rate is fixed at 32kHz and the divider in this register does not apply.

The sensor register output and FIFO output are both based on the Sample Rate.

When this register is effective under the *FCOICE_B* and *DLPF_CFG* settings, the reduced Sample Rate is generated by the formula below:

Sample Rate = Gyroscope Output Rate / (1 + *SMPLRT_DIV*)

where Gyroscope Output Rate = 1kHz.

Parameters:

SMPLRT_DIV 8-bit unsigned value. The Sample Rate is determined by dividing the gyroscope output rate by this value.

4.4 Register 26 – Configuration

CONFIG

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1A	26	-	FIFO_MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		

Description:

This register configures the FIFO's mode of operation, the external Frame Synchronization (FSYNC) pin sampling and the Digital Low Pass Filter (DLPF) setting. Please note that the DLPF can only be used when *FCHOICE_B*[1:0] =2b'00 (Register 27).

When *FIFO_MODE* is set to 1 and the FIFO is full, additional writes will not be written to the FIFO. When this bit is equal to 0 and the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data. In order to enable and disable writing to the FIFO, use the enable bits in Register 35. For further information regarding the FIFO's operation, please refer to Register 116.

An external signal connected to the FSYNC pin can be sampled by configuring *EXT_SYNC_SET*. Signal changes to the FSYNC pin are latched so that short strobes may be captured. The latched FSYNC signal will be sampled at the Sampling Rate, as defined in register 25. After sampling, the latch will reset to the current FSYNC signal state.

The sampled value will be reported in place of the least significant bit in a sensor data register determined by the value of *EXT_SYNC_SET* according to the following table.

EXT_SYNC_SET	FSYNC Bit Location
0	Input disabled
1	TEMP_OUT_L[0]
2	GYRO_XOUT_L[0]
3	GYRO_YOUT_L[0]
4	GYRO_ZOUT_L[0]

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B*[1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in the table below.

FCHOICE_B		DLPF_CFG	Gyroscope			Temperature Sensor	
<1>	<0>		Bandwidth (Hz)	Delay (ms)	Fs (kHz)	Bandwidth (Hz)	Delay (ms)
0	0	0	250	0.97	8	4000	0.04
0	0	1	184	2.9	1	188	1.9
0	0	2	92	3.9	1	98	2.8
0	0	3	41	5.9	1	42	4.8
0	0	4	20	9.9	1	20	8.3
0	0	5	10	17.85	1	10	13.4
0	0	6	5	33.48	1	5	18.6
0	0	7	3600	0.17	8	4000	0.04
x	1	x	8800	0.064	32	4000	0.04
1	0	x	3600	0.11	32	4000	0.04

Bit 7 is reserved.

Parameters:

FIFO_MODE	When set to 1 and the FIFO is full, additional writes will not be written to the FIFO. When equal to 0 and the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data. In order to disable writing to the FIFO, use the enable bits in Register 35.
EXT_SYNC_SET	3-bit unsigned value. Configures the FSYNC pin sampling.
DLPF_CFG	3-bit unsigned value. Configures the DLPF setting.

4.5 Register 27 – Gyroscope Configuration GYRO_CONFIG

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1B	27	XG_ST	YG_ST	ZG_ST	FS_SEL[1:0]		-	FCHOICE_B[1:0]	

Description:

This register is used to trigger gyroscope self test and configure the gyroscopes' full scale range.

Gyroscope self-test permits users to test the mechanical and electrical portions of the gyroscope. When self-test is activated by setting XG_ST, YG_ST, ZG_ST bits in register 27, the on-board electronics will actuate the appropriate sensor. This actuation will move the sensor's proof masses over a distance equivalent to a pre-defined Coriolis force. This proof mass displacement results in a change in the sensor output, which is reflected in the output signal. The output signal is used to observe the self-test response. The self-test response (STR) is stored in the sensor data output registers 67 – 72. This self-test-response is used to determine whether the part has passed or failed self-test

This self-test response must be within the limits provided in product specification document for the part to pass self-test. Otherwise, the part is deemed to have failed self-test.

FS_SEL selects the full scale range of the gyroscope outputs according to the following table.

FS_SEL	Full Scale Range
0	± 500 °/s
1	± 1000 °/s
2	± 2000 °/s
3	± 4000 °/s

FCHOICE_B, in conjunction with *DLPF_CFG* (Register 26), is used to choose the gyroscope output setting. For further information regarding the operation of *FCHOICE_B*, please refer to Section 4.2.

Bit 2 is reserved.

Parameters:

XG_ST	Setting this bit causes the X axis gyroscope to perform self test.
YG_ST	Setting this bit causes the Y axis gyroscope to perform self test.
ZG_ST	Setting this bit causes the Z axis gyroscope to perform self test.
FS_SEL	2-bit unsigned value. Selects the full scale range of gyroscopes.
FCHOICE_B	2-bit unsigned value used to choose the gyroscope output setting.

4.6 Register 35 – FIFO Enable
FIFO_EN

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23	35	TEMP_ FIFO_EN	XG_ FIFO_EN	YG_ FIFO_EN	ZG_ FIFO_EN	-	-	-	-

Description:

This register determines which sensor measurements are loaded into the FIFO buffer.

Data stored inside the sensor data registers (Registers 65 to 72) will be loaded into the FIFO buffer if a sensor's respective FIFO_EN bit is set to 1 in this register. The behavior of FIFO writes when the FIFO buffer is full can be configured with the *FIFO_MODE* bit (Register 26). In order to read the data in the FIFO buffer, the *FIFO_EN* bit (Register 106) must be enabled.

When a sensor's FIFO_EN bit is enabled in this register, data from the sensor data registers will be loaded into the FIFO buffer. The sensors are sampled at the Sample Rate as defined in Register 25. For further information regarding sensor data registers, please refer to Registers 65 to 72

Bits 3 through 0 are reserved.

Parameters:

TEMP_FIFO_EN	When set to 1, this bit enables TEMP_OUT_H and TEMP_OUT_L (Registers 65 and 66) to be written into the FIFO buffer.
XG_ FIFO_EN	When set to 1, this bit enables GYRO_XOUT_H and GYRO_XOUT_L (Registers 67 and 68) to be written into the FIFO buffer.
YG_ FIFO_EN	When set to 1, this bit enables GYRO_YOUT_H and GYRO_YOUT_L (Registers 69 and 70) to be written into the FIFO buffer.
ZG_ FIFO_EN	When set to 1, this bit enables GYRO_ZOUT_H and GYRO_ZOUT_L (Registers 71 and 72) to be written into the FIFO buffer.

4.7 Register 55 – INT Pin / Bypass Enable Configuration INT_PIN_CFG

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37	55	INT_LEVEL	INT_OPEN	LATCH _INT_EN	INT_RD _CLEAR	FSYNC_ INT_LEVEL	FSYNC _INT_ MODE_EN	-	-

Description:

This register configures the behavior of the interrupt signals at the INT pins. This register is also used to enable the FSYNC Pin to be used as an interrupt to the host application processor.

Bits 1 and 0 are reserved.

Parameters:

INT_LEVEL
When this bit is equal to 0, the logic level for the INT pin is active high.
When this bit is equal to 1, the logic level for the INT pin is active low.

INT_OPEN
When this bit is equal to 0, the INT pin is configured as push-pull.
When this bit is equal to 1, the INT pin is configured as open drain.

LATCH_INT_EN
When this bit is equal to 0, the INT pin emits a 50us long pulse.
When this bit is equal to 1, the INT pin is held high until the interrupt is cleared.

INT_RD_CLEAR
When this bit is equal to 0, interrupt status bits are cleared only by reading INT_STATUS (Register 58)

When this bit is equal to 1, interrupt status bits are cleared on any read operation.

FSYNC_INT_LEVEL
When this bit is equal to 0, the logic level for the FSYNC pin (when used as an interrupt to the host processor) is active high.
When this bit is equal to 1, the logic level for the FSYNC pin (when used as an interrupt to the host processor) is active low.

FSYNC_INT_MODE_EN
When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by *FSYNC_INT_LEVEL*. When a FSYNC interrupt is triggered, the *FSYNC_INT* bit in Register 58 will be set to 1. An interrupt is sent to the host processor if the FSYNC interrupt is enabled by the *FSYNC_INT_EN* bit in Register 56.

When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt.

4.8 Register 56 – Interrupt Enable

INT_ENABLE

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38	56	-	-	-	FIFO _OFLOW _EN	FSYNC _INT_EN	-	-	DATA _RDY_EN

Description:

This register enables interrupt generation by interrupt sources.

For information regarding the interrupt status for of each interrupt generation source, please refer to Register 58.

Bits 7 through 5, 2, and 1 are reserved.

Parameters:

FIFO_OFLOW_EN When set to 1, this bit enables a FIFO buffer overflow to generate an interrupt.

FSYNC_INT_EN When equal to 0, this bit disables the FSYNC pin from causing an interrupt to the host processor.

When set to 1, this bit enables the FSYNC pin to be used as an interrupt to the host processor.

DATA_RDY_EN When set to 1, this bit enables the Data Ready interrupt. The Data Ready interrupt is triggered when all the sensor registers have been written with the latest gyro sensor data.

4.9 Register 58 – Interrupt Status INT_STATUS

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3A	58	-	-	-	FIFO _OFLOW _INT	FSYNC _INT	-	-	DATA _RDY_INT

Description:

This register shows the interrupt status of each interrupt generation source. Each bit will clear after the register is read.

For information regarding the corresponding interrupt enable bits, please refer to Register 56.

Bits 7 through 5, 2, and 1 are reserved.

Parameters:

FIFO_OFLOW_INT This bit automatically sets to 1 when a FIFO buffer overflow interrupt has been generated.

The bit clears to 0 after the register has been read.

FSYNC_INT This bit automatically sets to 1 when an FSYNC interrupt has been generated.

The bit clears to 0 after the registers has been read.

DATA_RDY_INT This bit automatically sets to 1 when a Data Ready interrupt is generated.

The bit clears to 0 after the register has been read.

4.10 Registers 65 and 66 – Temperature Measurement TEMP_OUT_H and TEMP_OUT_L

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41	65	TEMP_OUT[15:8]							
42	66	TEMP_OUT[7:0]							

Description:

These registers store the most recent temperature sensor measurement.

Temperature measurements are written to these registers at the Sample Rate as defined in Register 25.

These temperature measurement registers, along with the gyroscope measurement registers, are composed of two sets of registers: an internal register set and a user-facing read register set.

The data within the temperature sensor's internal register set is always updated at the Sample Rate. Meanwhile, the user-facing read register set duplicates the internal register set's data values whenever the serial interface is idle. This guarantees that a burst read of sensor registers will read measurements from the same sampling instant. Note that if burst reads are not used, the user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready interrupt.

The scale factor and offset for the temperature sensor are found in the Electrical Specifications table in the Product Specification document.

Parameters:

TEMP_OUT 16-bit signed value.

Stores the most recent temperature sensor measurement.

4.11 Registers 67 to 72 – Gyroscope Measurements GYRO_XOUT_H, GYRO_XOUT_L, GYRO_YOUT_H, GYRO_YOUT_L, GYRO_ZOUT_H, and GYRO_ZOUT_L

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43	67	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT[7:0]							
47	71	GYRO_ZOUT[15:8]							
48	72	GYRO_ZOUT[7:0]							

Description:

These registers store the most recent gyroscope measurements. Gyroscope measurements are written to these registers at the Sample Rate as defined in Register 25.

The gyroscope sensor registers continuously update at the user selectable ODR sample rate whenever the serial interface is idle. It is recommended to use burst reads on host interface to guarantee a read of sensor registers will read measurements from the same sampling instant. Note that if burst reads are not used, the user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready interrupt. Failing to do so, may result in reading the low and high byte of the same sensor from different samples which could appear as noise peaks to the user for example. The following should be considered for single byte read mode:

1. Data_RDY_INT gets generated any time the sensor registers get updated with the sensor data. The frequency of this interrupt is the same as the ODR which is user selectable. The INT Configurations, INT status register and INT pin can be configured using the user register 37h, 38h and 3Ah.
2. The sensor register outputs are 16 bits (2 bytes). Both bytes should be read at the same time in order to get reliable data using burst mode. If a single byte read is used, the host needs to read the bytes back to back after Data_RDY_INT is set to ensure both bytes are from same sample.
3. The sensor registers should be read at a faster rate than the selected ODR with the read cycle preferably completed for all the sensors to get consistent and reliable output.

Each 16-bit gyroscope measurement has a full scale defined in *FS_SEL* (Register 27). For each full scale setting, the gyroscopes' sensitivity per LSB in *GYRO_xOUT* is shown in the table below:

FS_SEL	Full Scale Range	LSB Sensitivity
0	± 500 °/s	65.5 LSB/°/s
1	± 1000 °/s	32.8 LSB/°/s
2	± 2000 °/s	16.4 LSB/°/s
3	± 4000 °/s	8.2 LSB/°/s

Parameters:

GYRO_XOUT 16-bit 2's complement value.

Stores the most recent X axis gyroscope measurement.

GYRO_YOUT 16-bit 2's complement value.

Stores the most recent Y axis gyroscope measurement.

GYRO_ZOUT 16-bit 2's complement value.

Stores the most recent Z axis gyroscope measurement.

4.12 Register 106 – User Control

USER_CTRL

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6A	106	-	FIFO_EN	-	I2C_IF _DIS	-	FIFO _RESET	-	SIG_COND _RESET

Description:

This register allows the user to enable and disable the FIFO buffer and choose the primary I^2C interface. The FIFO buffer, sensor signal paths and sensor registers can also be reset using this register.

The primary SPI interface will be enabled in place of the disabled primary I^2C interface when *I2C_IF_DIS* is set to 1.

When the reset bits (*FIFO_RESET* and *SIG_COND_RESET*) are set to 1, these reset bits will trigger a reset and then clear to 0.

Bits 7, 5, 3, and 1 are reserved.

Parameters:

FIFO_EN When set to 1, this bit enables FIFO operations.

When this bit is cleared to 0, the FIFO buffer is disabled. The FIFO buffer cannot be read from while disabled. However, it can still be written to. In order to disable writing to the FIFO, please use the enable bits in Register 35.

The FIFO buffer's data will not be lost unless the FIFO is reset, or unless the device is power cycled or soft reset.

I2C_IF_DIS When set to 1, this bit disables the primary I^2C interface and enables the SPI interface instead.

FIFO_RESET This bit resets the FIFO buffer *w*hen set to 1. It is recommended that *FIFO_EN* be 0 when this is done. This bit automatically clears to 0 after the reset has been triggered.

SIG_COND_RESET When set to 1, this bit resets the signal paths for all sensors (gyroscopes and temperature sensor). This operation will also clear the sensor registers. This bit automatically clears to 0 after the reset has been triggered.

4.13 Register 107 – Power Management 1
PWR_MGMT_1

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6B	107	DEVICE _RESET	SLEEP	-	-	TEMP_DIS	CLKSEL[2:0]		

Description:

This register allows the user to configure the power mode and clock source. It also provides a bit for resetting the entire device, and a bit for disabling the temperature sensor.

By setting *SLEEP* to 1, the device can be put into low power sleep mode.

An internal 20MHz oscillator or the gyroscope based clock (PLL) can be selected as the device clock source. The PLL is the default clock source upon power up. In order for the gyroscope to perform to spec, the PLL must be selected as the clock source.

When the internal 20MHz oscillator is chosen as the clock source, the device can operate while having the gyroscopes disabled. However, this is only recommended if the user wishes to use the internal temperature sensor in this mode.

The clock source can be selected according to the following table.

CLKSEL	Clock Source
0	Internal 20MHz oscillator
1	PLL
2	PLL
3	PLL
4	PLL
5	PLL
6	Internal 20MHz oscillator
7	Reserved

For further information regarding the device clock source, please refer to the relevant Product Specification document and the Power Mode Transition Descriptions section in the Appendix.

Bits 5 and 4 are reserved.

Parameters:

DEVICE_RESET When set to 1, this bit resets all internal registers to their default values.
The bit automatically clears to 0 once the reset is done.
The default values for each register can be found in Section 3.

SLEEP When set to 1, this bit puts the device into sleep mode.

TEMP_DIS When set to 1, this bit disables the temperature sensor.

CLKSEL 3-bit unsigned value. Specifies the clock source of the device.

4.14 Register 108 – Power Management 2
PWR_MGMT_2

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6C	108	-	-	-	-	-	STBY_XG	STBY_YG	STBY_ZG

Description:

This register allows the user to put individual axes of the gyroscope into standby mode. Note that in order to activate any gyro axis again, all gyro axes must first be put into standby mode, and then be turned on simultaneously.

If the user wishes to put all three gyro axes into standby mode, the internal oscillator must be selected as the clock source (Register 107).

If all three gyro axes are put into standby mode while the clock source of the device is set to the PLL (with the gyro drive generating the reference clock), the chip will hang due to an absence of a clock. As long as one gyro axis is enabled, the drive circuit will remain active and the PLL will provide a clock.

Bits 7 through 3 are reserved.

Parameters:

STBY_XG When set to 1, this bit puts the X axis gyroscope into standby mode.

When cleared to 0 after all three gyro axes have been but into standby mode, the gyroscope turns on.

STBY_YG When set to 1, this bit puts the Y axis gyroscope into standby mode.

When cleared to 0 after all three gyro axes have been but into standby mode, the gyroscope turns on.

STBY_ZG When set to 1, this bit puts the Z axis gyroscope into standby mode.

When cleared to 0 after all three gyro axes have been but into standby mode, the gyroscope turns on.

4.15 Register 114 and 115 – FIFO Count Registers FIFO_COUNT_H and FIFO_COUNT_L

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
72	114	-	-	-	-	-	-	FIFO_COUNT[9:8]	
73	115	FIFO_COUNT[7:0]							

Description:

These registers keep track of the number of samples currently in the FIFO buffer in terms of the number of bytes stored.

These registers shadow the FIFO Count value. Both registers are loaded with the current sample count when FIFO_COUNT_H (Register 114) is read.

Note: Reading only FIFO_COUNT_L will not update the registers to the current FIFO COUNT value. FIFO_COUNT_H must be accessed first to update the contents of both these registers.

FIFO_COUNT should always be read in high-low order in order to guarantee that the most current FIFO Count value is read.

Bits 7 through 2 of Register 114 are reserved.

Parameters:

FIFO_COUNT 16-bit unsigned value. Indicates the number of bytes stored in the FIFO buffer. This number is in turn the number of bytes that can be read from the FIFO buffer and it is directly proportional to the number of samples available given the set of sensor data bound to be stored in the FIFO (register 35).

4.16 Register 116 – FIFO Read Write
FIFO_R_W

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
74	116	FIFO_DATA[7:0]							

Description:

This register is used to read and write data from the FIFO buffer.

Data is written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 65 through 72 will be written in order at the Sample Rate, based on the description for *SMPLRT_DIV*, located in Register 25.

The contents of the sensor data registers (Registers 65 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the treatment of the new data is determined by the *FIFO_MODE* bit in Register 26.

The user should check *FIFO_COUNT* to ensure that the FIFO buffer is not read when empty, and that more data than available is not read from the FIFO.

Parameters:

FIFO_DATA 8-bit data transferred to and from the FIFO buffer.

4.17 Register 117 – Who Am I
WHO_AM_I

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
75	117	-	WHO_AM_I[5:0]						-

Description:

This register is used to verify the identity of the device. The contents of *WHO_AM_I* are the upper 6 bits of the device's 7-bit I^2C address. The least significant bit of the devices' I^2C address is determined by the value of the AD0 pin. The value of the AD0 pin is not reflected in this register.

The default value of the register is 0x68.

Bits 0 and 7 are reserved. (Hard coded to 0)

Parameters:

WHO_AM_I Contains the 6-bit I^2C address of the gyroscope device

The Power-On-Reset value of Bit6:Bit1 is 110 100.

5 Appendix

5.1 Power Mode Transition Descriptions:

Note: “all gyros enabled” means that the *STBY_XG, STBY_YG*, and *STBY_ZG* bits in Register 108 all equal 0. Instructions should be followed in order.

1) Entering sleep mode
    a. Initially, any gyros enabled
    b. Set the *SLEEP* bit to 1
2) Exiting sleep mode:
    a. The chip is in sleep mode
    b. To exit sleep mode, first set *CLK_SEL* to 1
    c. Clear the *SLEEP* bit

Note: Because the *SLEEP* bit and *CLK_SEL* bit are in the same register, they can be set during the same write operation.

3) Put one or two gyros axes into standby
    a. Initially, all gyros enabled
    b. Put the desired gyro axes into standby by setting the *STBY_XG, STBY_YG*, or *STBY_ZG* bits
    c. The sense paths for the desired gyro axes are now in standby
4) Turn on one or two gyro axes from standby
    a. To re-enable any gyro axis, all axes must be enabled once at the same time. Thus, first put the part to sleep by setting the *SLEEP* bit
    b. Enable the desired axes by clearing the *STBY_XG, STBY_YG,* and *STBY_ZG* bits
    c. Exit sleep mode by clearing the *SLEEP* bit

Note: Alternatively, the user can first put all axes into standby mode, and then bring all the axes out of standby mode (see #5 and #6 below)

5) Put all gyro axes into standby mode (temp sensor only mode)
    a. Initially, all gyros enabled
    b. Select the internal oscillator as the clock source by setting *CLK_SEL* to 0. This is done because putting all the gyros into standby will disable the PLL. Meanwhile, the chip does not auto select the internal oscillator when this happens. Thus, the chip would hang (requiring a soft reset or a power cycle to remedy).
    c. Wait 20µs for the internal oscillator to stabilize
    d. Put all gyro axes into standby by setting the *STBY_XG, STBY_YG*, and *STBY_ZG* bits to 1
    e. The drive and sense paths for all axes, as well as the PLL are now off.
6) Turn on all gyros from standby mode
    a. To enable all axes, first set *CLK_SEL* to 1. The chip will continue to use the internal oscillator as the clock source until the PLL is ready, and will not hang
    b. Exit standby mode by clearing the *STBY_XG, STBY_YG*, and *STBY_ZG* bits to 0.
    c. Once the PLL is ready, the clock source will switch to the PLL

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