REV 1.4

Technical Description

IT310 GPS Receiver

This document describes the electrical connectivity and main functionality of the IT310 module.

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CHANGE LOG

Rev.	Notes	Date
0.1	Preliminary documentation	2007-01-25
0.2	Continued editing	2007-03-02
1.0	Added reference circuit drawing. Corrected table 6, TIMESYNC signal from GPIO13 to GPIO15. Updated Application Board to rev B. Added re-programming procedure.	2007-03-28
1.1	Clarified operation modes, updated soldering profile and other minor corrections, separated mechanical and pin out drawings	2007-08-22
1.2	Updated tape and reel drawing, updated reflow soldering temperature profile (removed picture)	2007-10-9
1.3	HW revision C: Updated specifications due to transition to SiRF GSC3e/LPx chip with 75mW power. Module name changed to IT310. Updated block diagram. I/O level change to 2.8V CMOS, inputs are 3.3V tolerable. XRESET & WAKEUP inputs are 1.2V CMOS compatible and 3.3V tolerable. Removed suggestion for external LNA usage with passive antenna.	2009-01-21
1.4	Corrections: Table 3 Connections (added missing pins 31-36, pull up/down value), section 4.4 Note (removed), ECLK and TIMSYNC input suggestion. Clarified soldering profile, added *ref 2*.	2009-06-09

CONTENTS

COMPLEMENTARY READING

The following reference documents are complementary reading for this document:

Ref. #	File name	Document name
1	SiRF low power modes	Application note on TricklePower and Push-to-Fix low power modes
2	Reflow_soldering_ profile.pdf	Soldering Profile

The following SiRF reference documents are also complementary reading for this document.

Ref. #	File name	Document name
I	GSC3LPxProductInsert.pdf	GSC3e(f)/LPx Product Insert
II	NMEA Reference Manual.pdf	NMEA Reference Manual
III	SiRF Binary Protocol Reference Manual.pdf	SiRF Binary Protocol Reference Manual
IV	APNT3008.pdf	SiRF Application Note Power Management Considerations of SiRFstarIII

1 GENERAL DESCRIPTION

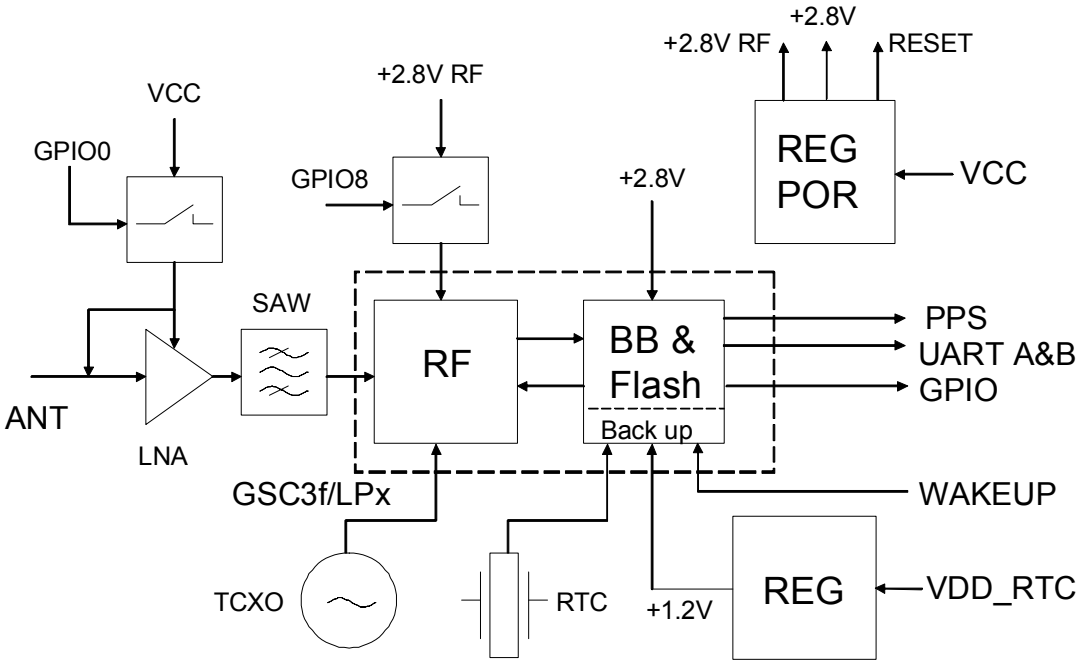
The Fastrax IT310 is an OEM GPS receiver module, which provides the SiRFstarIII receiver *(ref I)* functionality using the low power SiRF GSC3f/LPx chip. The module has tiny form factor 13.1x15.9mm, height is 2.3mm nominal (2.6mm max). The IT310 receiver provides low power and very fast TTFF together with weak signal acquisition and tracking capability to meet even the most stringent performance expectations. The module is available with SiRF GSW3 firmware.

The module provides complete signal processing from antenna to serial data output in either NMEA messages *(ref II)* or in SiRF binary protocol *(ref III)*. A second serial port is also available for custom purposes. The module requires a main power supply VCC, a back up supply voltage VDD_RTC for non-volatile RTC & RAM blocks and GPS antenna input signal.

The IT310 module interfaces to the customer's application via two serial ports, two control signals, PPS timing signal and programmable GPIO signals. Serial data and all I/O signal levels are CMOS compatible. The antenna input supports passive and active antennas and provides also an internally generated antenna bias supply.

This document describes the electrical connectivity and main functionality of the IT310 hardware.

1.1 Block diagram



1.2 Frequency Plan

Clock frequencies generated internally at the IT310 receiver:

- 32768 Hz real time clock (RTC)

- 16.369 MHz master clock (TCXO)
- 1571.424 MHz local oscillator of the RF down-converter

2 SPECIFICATIONS

2.1 General

Table 1 General specifications

Receiver	GPS L1 C/A-code, SPS
Channels	20 physical (12 in tracking, firmware limited)
Update rate	1 Hz default (fix rate configurable with SiRF TricklePower)
Supply voltage, VCC	+3.0V…+3.6 V
Back up supply voltage, VDD_RTC	+1.5V…+3.6 V (preferably active all the time)
Power consumption, VCC	75 mW typical @ 3.0V (without Antenna bias)
Power consumption, VDD_RTC	18 uW typical @ 3.0V (during Back up state)
Antenna net gain range	0…+35dB (+10… +35dB suggested for optimum performance)
Antenna bias voltage	Same as VCC
Antenna bias current	150 mA max (must be externally limited at VCC)
Storage temperature	-40ºC…+85ºC
Operating temperature	-30ºC…+85ºC (*note 1*)
Serial port configuration (default)	Port A: NMEA; Port B: no protocol
Serial data format	8 bits, no parity, 1 stop bit
Serial data speed (default)	NMEA: 9600 baud
I/O signal levels	GPIO, UART: 2.8V CMOS compatible: low state 0…0.8V; high state 2.0…2.8V. Inputs are 3.3V tolerable (excluding ECLK input). XRESET, WAKEUP: 1.2V CMOS compatible: low state 0…0.3V; high state 0.9… 1.2V. Inputs are 3.3V tolerable.
I/O sink/source capability	+/- 2 mA max.
PPS output	+/-1us accuracy

Note 1: Usage in the temperature range –40°C… –30°C is accepted but Time-to-First-Fix may be increased.

2.2 Absolute maximum ratings

Table 2 Absolute maximum ratings

Item	Min	Max	unit
Operating and storage temperature	-40	+85	ºC
Power dissipation	-	500	mW
Supply voltage, VCC	-0.3	+3.6	V
Supply voltage, VDD_RTC	-0.3	+5.5	V
Current output on antenna input	0	+150	mA
Input voltage on any input connection except ECLK	-0.3	+3.6V	V
Input voltage at ECLK input	-0.3	+3.1	V
RF input level	-	+15	dBm

3 OPERATION

3.1 Operating modes

After power up IT310 boots from the internal flash memory for normal operation. Modes of operation:

- Normal (Navigating) mode
    - Back up state
    - Power management system modes (TricklePower, Push-to-Fix)
- Programming mode

3.2 Normal mode

The IT310 receiver enters navigating mode after power up. It will start navigation automatically after power up/reset using all (if any) aiding information on GPS time, satellite ephemeris and Last Known Good (LKG) position information provided by the non-volatile back up block (RTC & RAM). The power consumption will vary depending on the amount of satellite acquisitions and number of satellites in track. This mode is also referenced as Full-power state.

Navigation is available as long as the VCC and VDD_RTC power supplies are active. Any configuration settings are valid as long as the back up supply VDD_RTC is active. When the VDD_RTC is powered off, the configuration is reset to default configuration on next power up.

3.2.1 Firmware configuration

Fastrax default SiRF GSW3 firmware configuration *(ref III)*, firmware variant ***CAR***:

1. Port A: NMEA 9600 baud
2. NMEA output: GGA, RMC, GSV, GSA (all 1 sec interval)
3. Port B: no protocol
4. Track smoothing: disabled
5. Static navigation: enabled
6. DGPS/SBAS: disabled
7. Datum: WGS84

3.3 Back up state

Back up mode means a low quiescent power state where only the internal non-volatile RTC and RAM block is powered on via VDD_RTC supply. The main supply input VCC is powered off and navigation is halted.

When the main supply VCC is powered on again, the receiver will start navigation automatically with fastest possible TTFF using all (if any) aiding information on GPS time, satellite ephemeris and Last Known Good (LKG) position information provided by the non-volatile back up block (RTC & RAM).

3.4 Power management modes

The receiver supports also SiRF operating modes for reduced average power consumption (*ref IV*) like Adaptive TricklePower™ and Push-to-Fix™ modes:

1. *Adaptive TricklePower:* In this mode the receiver stays at Full Power for 200… 900ms and provides a valid fix. Between fixes with 1… 10 sec interval the receiver stays in a low power Stand-by state to reduce power drain. TricklePower mode is configurable with SiRF binary protocol message ID151 (*ref III*). The receiver stays once in while in Full Power automatically to collect new ephemeris and almanac data from rising satellites.

2. *Push-to-Fix*: In this mode the receiver is configured to wake up periodically, typically every 1800 sec, to collect new ephemeris data from rising satellites. Rest of the time the receiver stays in a low power CPU only state. The host wakes up the receiver by ON_OFF control input interrupt (pulse low-high-low >62us) after which the receiver performs Hot start and a valid fix is available within few seconds. This mode is configurable with SiRF binary protocol message ID151 (*ref III*).

Note that position accuracy is somewhat degraded in power management modes when compared to full power operation.

3.5 Programming mode

Re-programming via HW-booting mode is utilized by keeping the BOOTSEL control input at high state during power up or at system reset. Now the GPS module boots from the serial data Port A and waits for the boot loader commands from the host (an application running on the host, SiRFFlash). It is suggested that all applications should support the HW-booting by access to serial Port A (TX & RX), BOOTSEL and XRESET signals.

Note that during the flash update process the serial data speed is changed and thus the serial line connection should be a direct line to the host without any transferring utilities that may cause a failure during speed change.

3.6 Procedure for re-programming the firmware

This procedure assumes Fastrax Evaluation kit with IT310 application board.

1. Connect serial Port A (Port 0) to PC.

2. Set the module to UART boot mode: Power up the module with BOOTSEL signal high. Alternatively give a XRESET pulse high-low-high while keeping BOOTSEL signal high after the power supply is on. With iTrax Evaluation Kit press the front panel Prog/Reset switch once to Prog position.

3. Start SiRFFlash application on PC.

4. Browse for the flash *.s file.

5. Check the Communication setting from the SiRFFlash to meet your PC serial port.

6. Press Execute at SiRFFlash. Now the flashing starts.

7. After flashing has finished, recover normal operation by booting the module normally with BOOTSEL low. With iTrax Evaluation Kit press the Prog/Reset switch once to Reset position.

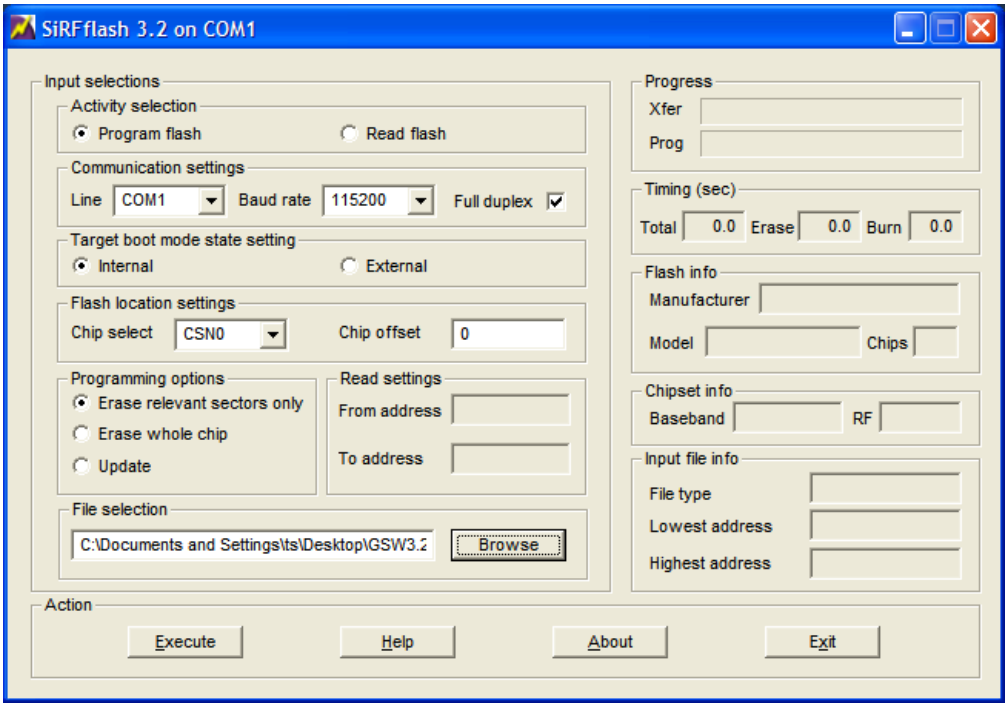


Figure 1 SiRFFlash utility settings

4 CONNECTIVITY

4.1 Connection assignments

The I/O connections are available as soldering pads on the bottom side of the module. These pads are also used to attach the module on the motherboard in application. All the unconnected I/O can be left open (floating) unless instructed externally to use pull up or pull down.

Table 3 Connections

Contact	Signal name	I/O	Alternative signal name	Signal description
1	ANT	I/O	-	Antenna signal input, Antenna bias voltage output
2	GND	-	-	Ground
3	GND	-	-	Ground
4	GND	-	-	Ground
5	VDD_RTC	I	-	Power supply for battery back up
6	GND	-	-	Ground
7	BOOTSEL	I	-	Boot control input: 1 = UART for re-programming; 0 = Internal flash memory. Input is pulled low internally with 100kohm resistor (3)
8	GND	-	-	Ground
9	GND	-	-	Ground
10	GND	-	-	Ground
11	VCC	I	-	Power supply
12	GND	-	-	Ground
13	XRESET	I	-	Asynchronous system reset, active when low 0… 0.3V. Pulled internally high to VCC with 100kohm resistor. (4)
14	GND	-	-	Ground
15	GND	-	-	Ground
16	ECLK	I	-	Option for external clock input. Not used with GSW3 firmware. Input is CMOS 2.8V compatible, *not* 3.3V tolerable. (2)
17	GND	-	-	Ground
18	GPIO1	I/O	Odometer Input	Not used with GSW3 firmware. GPIO signal (2) (3)

19	GND	-	-	Ground
20	PPS	O	GPIO9	1PPS signal output (2) (3)
21	GND	-	-	Ground
22	GND	-	-	Ground
23	GND	-	-	Ground
24	GND	-	-	Ground
25	TIMESYNC	I	GPIO15	Option for Timesync input. Not used with GSW3 firmware. (1) (3)
26	GND	-	-	Ground
27	WAKEUP	I	ON_OFF	ON_OFF control input for wakeup from Hibernate/Stand-by states: low-to-high-low pulse >62us. Can be used only to wake up from Push-to-Fix operation. Pull low externally with 4k7 to 10k resistor. (4)
28	GND	-	-	Ground
29	GND	-	-	Ground
30	TXA	O	-	UART A async. output (3)
31	RXA	I	-	UART A async. input (1) (3)
32	RXB	I	-	UART B async. input (1) (3)
33	GND	-	-	Ground
34	TXB	O	-	UART B async. output (3)
35	GND	-	-	Ground
36	GND	-	-	Ground
Contact	Signal name	I/O	Alternative GPIO name	Signal description

Notes:

(1) Has internal 30kohm (nom.) pull up resistor to +2.8V. Input can be left unconnected if not used.

(2) Has internal 30kohm (nom.) pull down resistor to GND. Input can be left unconnected if not used.

(3) +2.8V CMOS compatible signal levels. Input is +3.3V tolerable.

(4) +1.2V CMOS compatible signal levels. Input is +3.3V tolerable.

4.2 Power supply

The IT310 module requires two separate power supplies: VDD_RTC for non-volatile back up block (RTC/RAM) and the VCC for digital parts and I/O. RF and digital sections have internally regulated +2.8V supplies. VCC can be switched off when navigation is not needed but if possible keep the back up supply VDD_RTC active all the time in order to keep the non-volatile RTC & RAM active for fastest possible TTFF.

Back up supply VDD_RTC draws typically 6uA current in back up state. During navigation VDD_RTC current may peak typically up to 70uA.

Main power supply VCC current varies according to the processor load and satellite acquisition. Typical VCC peak current is 32mA during acquisition after power up.

Both power inputs have internal ceramic, low ESR capacitors. Use a power supply or regulator that is compatible with low ESR (~ 0.01 ohm) ceramic output load capacitors.

NOTE

Use a power supply or regulator that is compatible with low ESR (~ 0.01 ohm) ceramic output load capacitors.

4.3 Reset

The reset input XRESET is an active low asynchronous reset. The processor boots after the low-to-high transition depending on the state of the BOOT signal. The XRESET input contains an internal voltage detector to force reset during power up or power down transitions.

The input has internal 100k pull up resistor to VDD. For normal operation the XRESET input can be left unconnected.

NOTE

XRESET input is CMOS 1.2V compatible. For proper reset pull input below 0.3V. The input is 3.3V tolerable and is pulled high with internal 100kohm resistor to VCC.

4.4 Boot Select

The boot source is defined in the internal boot ROM sector by using the BOOTSEL control input. After power up or after system reset the value is read and the boot is processed according the following table.

Table 4 Boot select

BOOTSEL	I/O	Boot source
LOW	I	Boot for internal flash memory (Normal operation)

HIGH	I	External boot UART Port A for re-programming

The input has internal 100kohm pull down resistor and can be left unconnected if not used. Boot select should be kept valid after power up for at least 500 ms to allow the internal power-on-reset delay to settle.

In Navigating mode the Boot Select should be kept valid for at least 10us after XRESET low-to-high transition.

4.5 WAKEUP control input

The module can be controlled to wake up from Push-to-Fix low power mode by the WAKEUP control input (internally named as ON_OFF signal). The wake up interrupt is generated by a low-high-low toggle, which should be longer than 62us.

NOTE

If not used, pull WAKEUP signal externally to low state.

4.6 ELCK

The ECLK is available optionally for external clock input with the SiRFLoc firmware. The input is 2.8V CMOS compatible and can be left unconnected. Note that the input is *not* 3.3V tolerable as other inputs. Max input voltage is +3.1V.

4.7 Antenna input

The module supports passive and active antennas. The antenna input impedance is 50 ohms. During normal (navigating) operation, the input provides also a bias supply (the same as VCC). When the navigation is stopped, the antenna bias is switched off internally.

The maximum tolerated antenna bias current is 150mA, which shall be current limited by the external regulator supplying VDD.

NOTE

Passive antennas with a short-circuit to GND should be DC blocked externally with a 18pF…1nF serial capacitor.

4.7.1 Active GPS antenna

The customer may use an external active GPS antenna for e.g. in mobile or indoor usage. It is suggested the active antenna has a net gain *including cable loss* in the range from +10 dB to +35 dB.

Antenna bias supply has no internal short circuit protection. The maximum tolerated antenna bias current is 150mA, which should be current limited by the external regulator supplying VCC. Applications that require smaller than 150mA antenna bias short circuit protection should use an external antenna bias circuit with suitable current limiting.

NOTE

Antenna bias current from VCC supply should be limited externally to 150 mA max.

4.8 UART

The device supports UART communication via Port A and Port B. With the standard firmware the Port A is configured by default to NMEA protocol with 9600 baud and Port B is set to 'no protocol'. The Port A is used also when the device is booting from the serial port.

The default configuration for Ports and respective protocols can be changed by commands via NMEA or SiRF binary protocols *(ref II & III)*. Any custom configuration stays active as long as the back up supply VDD_RTC is active.

I/O levels form the serial ports are 2.8V CMOS compatible, not RS232 compatible. Use an external level converter to provide RS232 levels when needed. Inputs are 3.3V tolerable.

4.9 Dedicated GPIO

Some of the GPIOs have a shared or dedicated functionality. Each signal is named according to the main functionality but also the secondary functionality is listed as the Alternative signal name.

All GPIO's are configured to inputs by default after system reset. I/O levels from GPIO are 2.8V CMOS compatible and inputs are 3.3V tolerable.

4.9.1 GPIO1

GPIO1 is available externally for custom purposes.

4.9.2 PPS/GPIO9

The pulse-per-second (PPS) output provides an output for timing purposes. It shares the PPS functionality with GPIO9 for custom purposes.

4.9.3 TIMESYNC/GPIO15

The TIMESYNC is available optionally for external timing input with the SiRFLoc firmware and can be left unconnected. A timing pulse is triggered on the rising edge, minimum 100ns wide, maximum ~1ms. It can be used also for GPIO usage with custom firmware.

4.10 Mechanical dimensions and contact numbering

Module size is 13.1mm (width) x 15.9mm (length) x 2.3mm (height 2.6mm max). General tolerance is ±0.3mm.

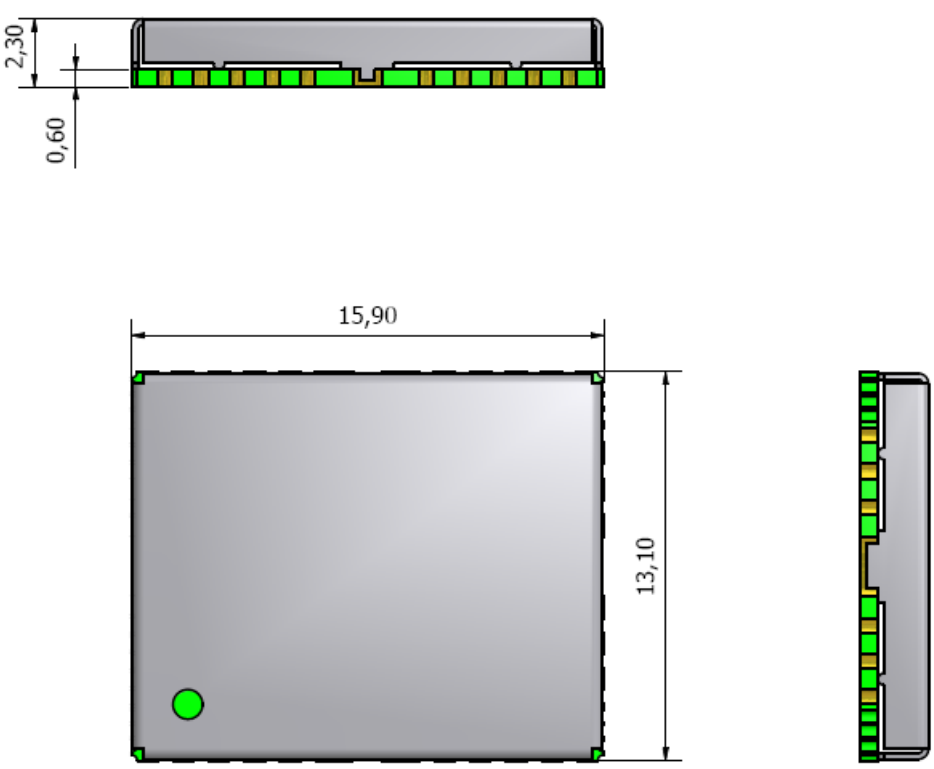


Figure 2 Dimensions

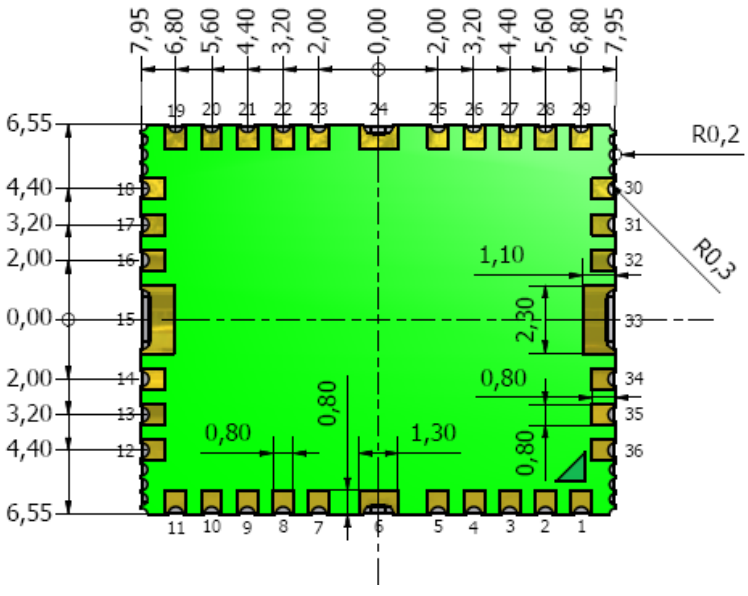


Figure 3 Contact numbering, bottom view.

4.11 Suggested pad layout

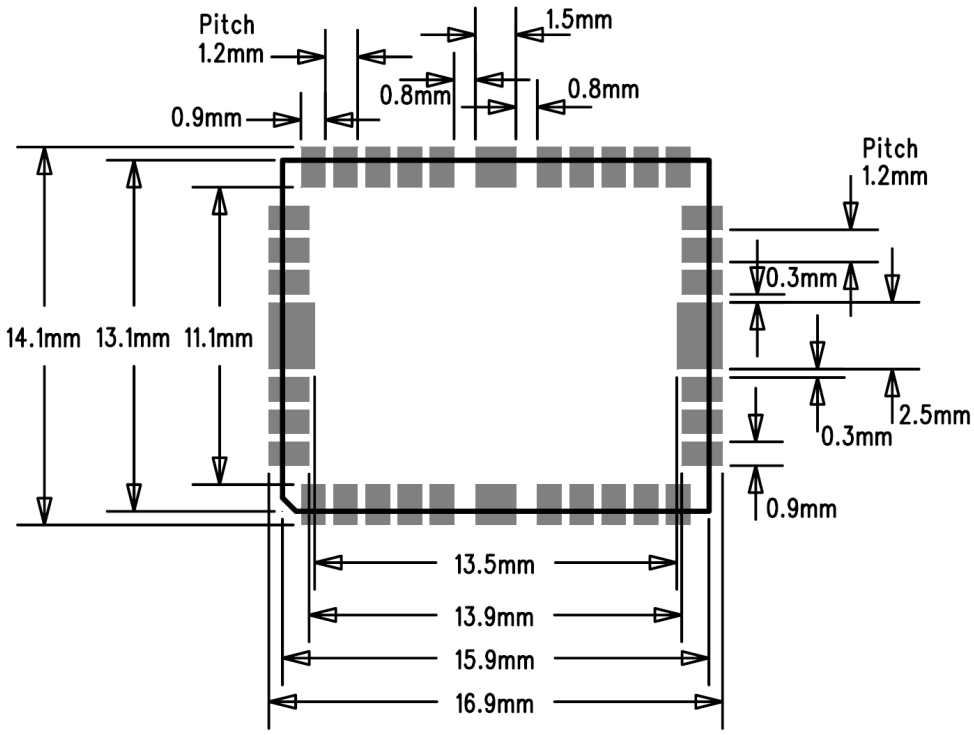


Figure 4 Suggested pad layout and occupied area, top view.

5 MANUFACTURING

5.1 Assembly

The IT310 module supports only assembly and soldering in a reflow process on the top side of the PCB. Suggested solder paste stencil height is 150um minimum to ensure sufficient solder volume.

5.2 Suggested Reflow soldering profile

Use pre-heating at 150… 180 ºC for 60… 120 sec. Suggested peak reflow temperature is 235… 245ºC (for SnAg3.0Cu0.5 alloy). Absolute max reflow temperature is 260ºC. For details see Fastrax document 'Soldering Profile' (*ref 2*).

5.3 Moisture sensitivity

Note that the IT310 is moisture sensitive at MSL 3 (see the standard IPC/JEDEC J-STD-020C). The module must be stored in the original moisture barrier bag or if the bag is opened, the module must be repacked or stored in a dry cabin (according to the standard IPC/JEDEC J-STD-033B). Factory floor life in humid conditions is 1 week for MSL 3.

5.4 Tape and reel

One reel contains 500 modules.

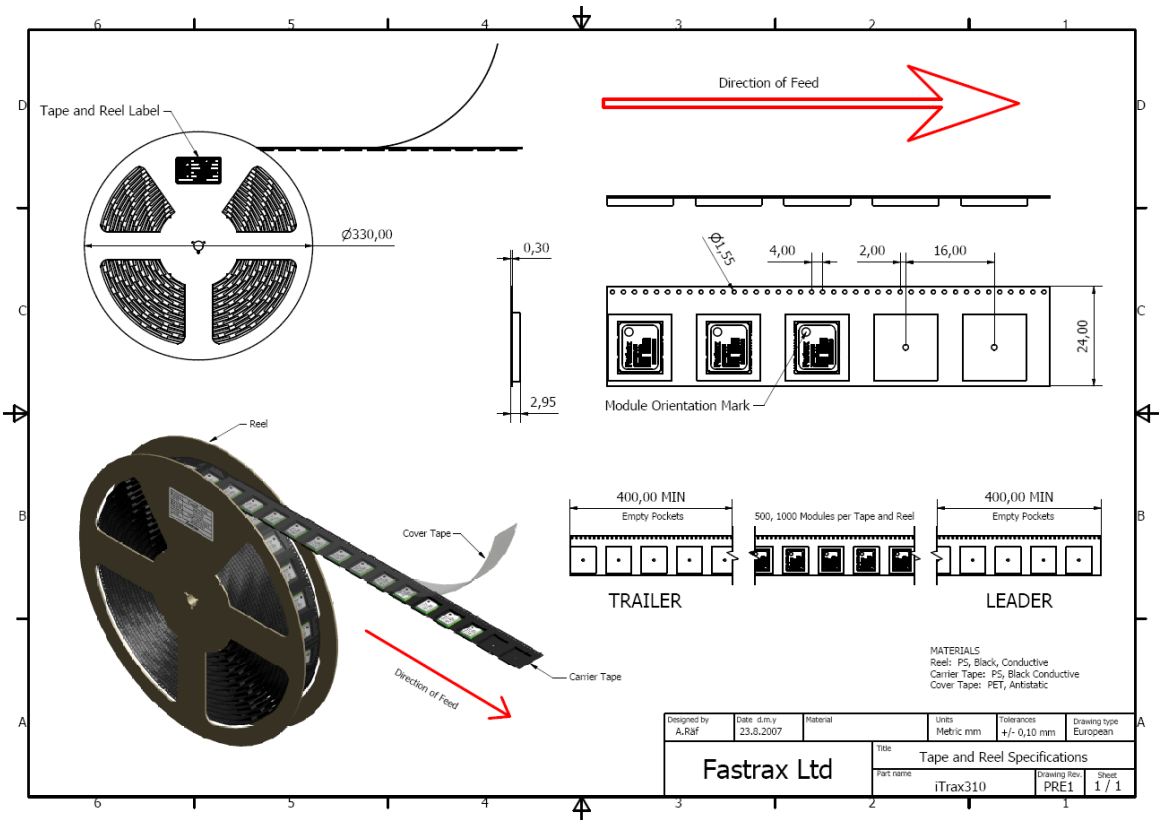


Figure 5 Tape and reel specification

6 REFERENCE DESIGN

The idea of the reference design is to give a guideline for the applications using the IT310 GPS module. In itself it is not a finished product, but an example that performs correctly.

In the following two chapters the reader is exposed to design rules that he should follow, when designing an IT310 in to the application. By following the rules one end up having an optimal design with no unexpected behavior caused by the PCB layout itself. In fact these guidelines are quite general in nature, and can be utilized in any PCB design related to RF techniques or to high speed logic.

Note that there is a DC bias voltage present at the RF input, when the module is operating in Navigating mode. If a passive antenna with a short-circuit to the GND is used, an external series DC block capacitor (18pF…1nF) must be used for the RFIN signal line.

6.1 Reference circuit diagram

The following picture describes a minimum connectivity for a typical autonomous navigation application. It consists of the IT310 module, which is powered by the main VCC supply (+3.0… +3.3V range) and which can be controlled on/off by the host.

The back up supply VDD_RTC is provided by the rechargeable Lithium coin cell battery BT1. It has associated components for re-charging (R9, R12 and D1). R9 can be omitted when VCC is below $\leq$ +3.2V. BT1, R9, R12 and D1 can be also replaced with a suitable back up supply if such is available in the application.

Serial port TXA is connected to host UART input. RXA connection to host UART output is required when sending commands to IT310.

Optional connectivity includes PPS signal for timing purposes, XRESET and BOOTSEL control signal for e.g. re-programming the firmware.

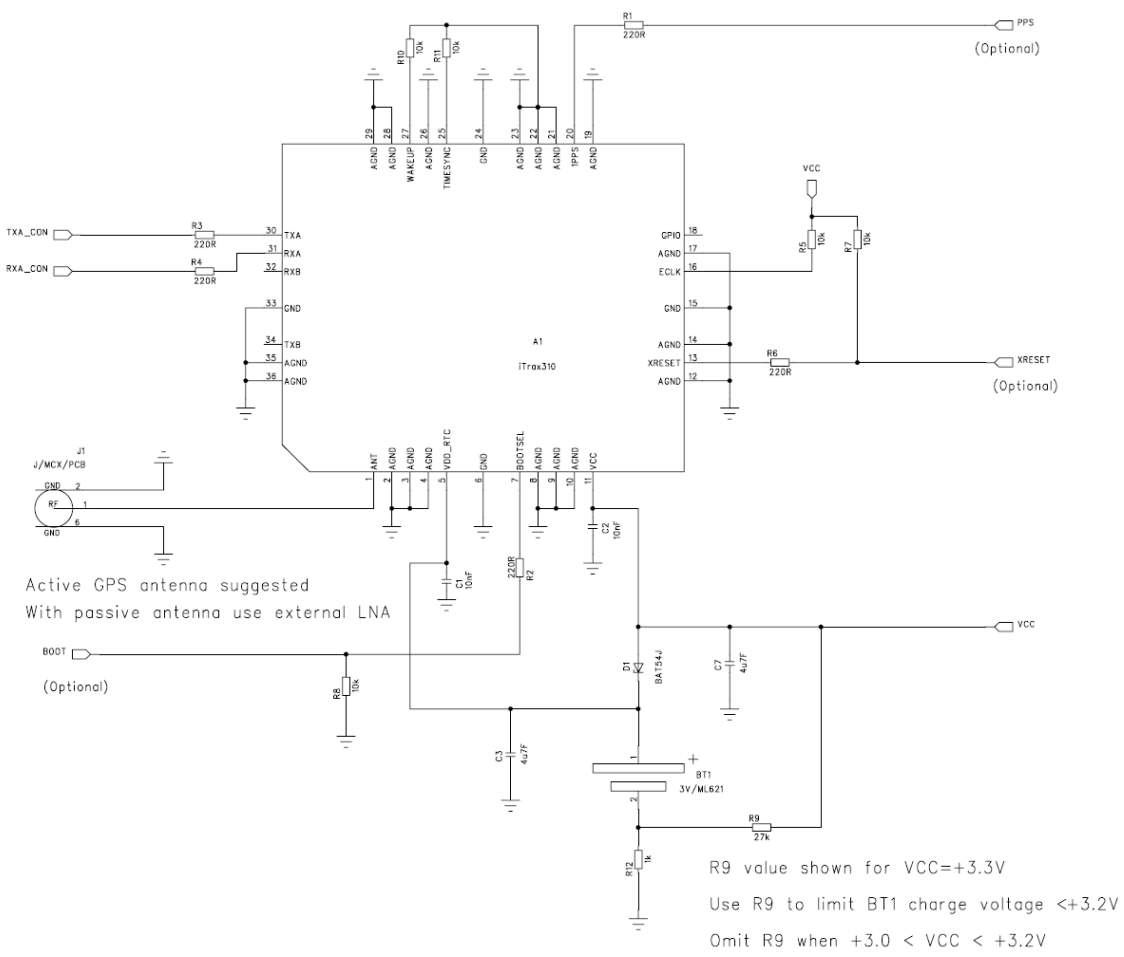


Figure 6 Reference Circuit Drawing

6.2 PCB layout issues

The suggested 4-layer PCB build up is presented in the following table.

Table 5 Suggested PCB build up

Layer	Description
1	Signal + Ground with copper keep-out below IT310
2	Ground plane
3	Signal + Ground or VCC plane
4	Signal (short traces) + Ground

Routing signals directly under the module should be avoided. This area should be dedicated to keep-out to both traces and to ground (copper), except for via holes, which can be placed close to the pad under the module. If possible, the amount of VIA holes underneath the module should be also minimized.

For a multi-layer PCB the first inner layer below the IT310 is suggested to be dedicated for the ground plane. Below this ground layer other layers with signal traces are allowed. It is always better to route very long signal traces in the inner layers of the PCB. In this way the trace can be easily shielded with ground areas from above and below.

The serial resistors at the I/O should be placed very near to the IT310 module. In this way the risk for the local oscillator leakage is minimized. For the same reason by-pass capacitors C1 and C2 should be connected very close to the module with short traces to IO contacts and to the ground plane. Place the GND via hole as close as possible to the capacitor.

Connect the GND soldering pads of the IT310 to ground plane with short traces to via holes, which are connected to the ground plane. Use preferably two via holes per GND pad.

The RF input should be routed clearly away form other signals, this minimizes the possibility of interference. The proper width for the 50 ohm transmission line impedance depends on the dielectric material of the substrate and on the height between the signal trace and the first ground plane. With FR-4 material the width of the trace shall be two times the substrate height.

A board space free of any traces should be covered with copper areas (GND). In this way, a solid RF ground is achieved throughout the circuit board. Several via holes should be used to connect the ground areas between different layers.

Additionally, it is important that the PCB build-up is symmetrical on both sides of the PCB core. This can be achieved by choosing identical copper content on each layers, and adding copper areas to route-free areas. If the circuit board is heavily asymmetric, the board may bend during the PCB manufacturing or reflow soldering. Bending may cause soldering failures.

7 IT310 APPLICATION BOARD

The IT310 Application Board provides the IT310 connectivity to the Fastrax Evaluation Kit or to other evaluation purposes. It provides a single PCB board equipped with the IT310 module, one regulator for VCC supply, a Li-Ion battery for VDD_RTC back up supply, an MCX antenna connector, an option to assemble a LNA circuit before the antenna input and a 2x20 pin Card Terminal connector.

7.1 Card Terminal I/O-connector

The following signals are available at the 40-pin Card Terminal I/O connector J2. The same pin numbering applies also to the iTrax Evaluation Kit pin header J4. Note that serial Port A and B maps to Port 0 and 1 at the Evaluation Kit, respectively.

Table 6 IT310 Application Board connectivity

Pin	Signal name	I/O	Alternative GPIO	Interface to Fastrax Evaluation Kit
1	TXB_CON	O	-	UART 1 async. output
2	GND	-	-	Ground
3	RXB_CON	I	-	UART 1 async. input
4	GND	-	-	Ground
5	TXA_CON	O	-	UART 0 async. output
6	GND	-	-	Ground
7	RXA_CON	I	-	UART 0 async. input
8	GND	-	-	Ground
9	VDD_CON	I	-	Power input +3.3V
10	GND	-	-	Ground
11	PPS_CON	O	GPIO9	1PPS signal output
12	GND	-	-	Ground
13	XRESET_CON	I	-	Active low async. system reset
14	-	-	-	Not connected
15	-	-	-	Not connected
16	BOOT1_CON	I	-	Boot Select
17	GND	-	-	Ground
18	-	-	-	Not connected

19	-	-	-	Not connected
20	-	-	-	Not connected
21	GND	-	-	Ground
22	-	-	-	Not connected
23	ON_OFF	I	-	ON_OFF control input
24	-	-	-	Not connected
25	GND	-	-	Ground
26	GPIO1	I/O	-	GPIO1 pin
27	-	-	-	Not connected
28	TIMESYNC	I	GPIO15	Timesync input
29	-	-		Not connected
30	-	-	-	Not connected
31	GND	-	-	Ground
32	-	-	-	Not connected
33	GND	-	-	Ground
34	-	-	-	Not connected
35	GND	-	-	Ground
36	-	-	-	Not connected
37	GND	-	-	Ground
38	-	-	-	Not connected
39	GND	-	-	Ground
40	ECLK	I	-	ECLK clock input
Pin	Signal name	I/O	Alternative GPIO	Interface to Fastrax Evaluation Kit

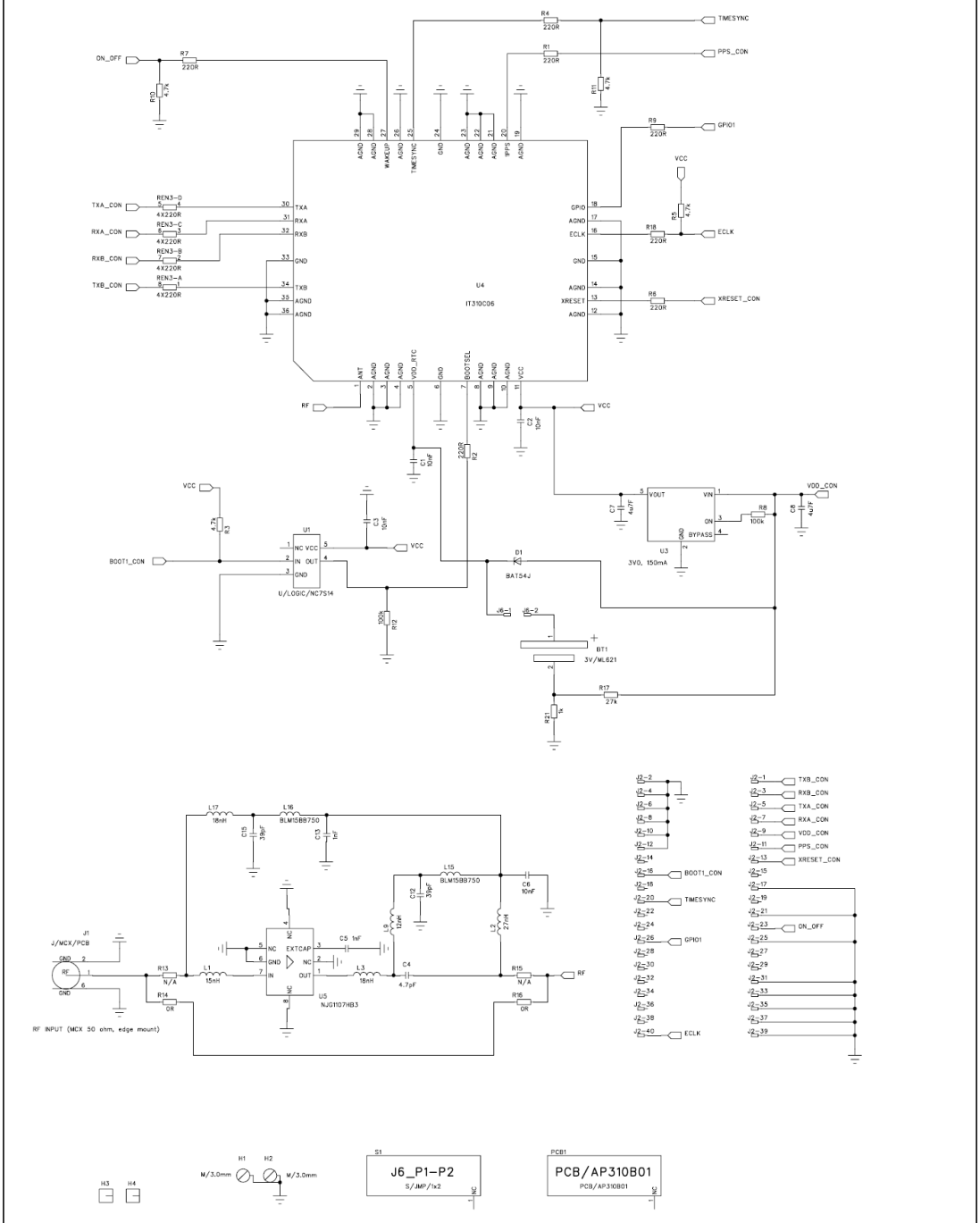
7.2 Bill of materials

Item	Reference	Part Name	Description
1	BT1	3V/ML621	PANASONIC ML621/F9D, 3V 5mAh
2	C15	18pF	Capacitor chip, 18pF 50V 5% NP0 0402
3	C4	4.7pF	4.7pF 50V +-0.25pF (5%) NP0 0402 Capacitor chip
4	C1	10nF	10nF 16V 10% X7R 0402
5	C6	10nF	10nF 16V 10% X7R 0402
6	C2	10nF	10nF 50V 10% X7R 0402
7	C3	10nF	10nF 50V 10% X7R 0402
8	C5	1nF	Capacitor chip, 1nF 50V 10% X7R 0402
9	C12	1nF	1nF 50V 10% X7R 0402 Capacitor chip
10	C13	1nF	Capacitor chip, 1nF 50V 10% X7R 0402
11	C7	4u7F	4,7uF 6,3V X5R 0805 +-20%
12	C8	4u7F	4,7uF 6,3V X5R 0805 +-20%
13	D1	BAT54J	Diode 75V 225mA, BAT54J
14	H3	FIDUCIAL	FIDUCIAL, Circle, rectangle, triangle
15	H4	FIDUCIAL	FIDUCIAL, Circle, rectangle, triangle
16	H1		
17	H2		
18	U4	IT310A06	iTrax310 rev A, Drill cut panel
19	J6	1x2P2.54	1x2 pin-header, straight, 2,54mm
20	J2	2x20 EDGE	EDGE MOUNT SOCKET STRIP 40 PINS
21	J1	CON/BNC_90DEG_PCB	50 Ohm male MCX connector PCB
22	L9	12nH	Coil chip, 12nH 0402 +-5%, 300mA Q:8 0.41 DCR
23	L1	15nH	Coil chip, 15nH 0402 +-5%, 300mA Q:8 0.33 DCR
24	L3	18nH	Coil chip, 18nH 0402 +-5%, 300mA Q:8 0.51 DCR
25	L17	18nH	Coil chip, 18nH 0402 +-5%, 300mA Q:8 0.51 DCR
26	L2	27nH	Coil chip, 27nH 0402 +-5%,
27	L15	BLM15BB750	75R,+-25%@100MHz, 0R4@DC, 300mA
28	L16	BLM15BB750	75R,+-25%@100MHz, 0R4@DC, 300mA
29	PCB1	PCB/AP310B01	Application board for PCB iTrax310, Rev. B
30	R13	N/A	Resistor chip, 0R 0402
31	R14	0R	Resistor chip, 0R 0402
32	R15	N/A	Resistor chip, 0R 0402
33	R16	0R	Resistor chip, 0R 0402
34	R8	100k	100k 5% 0402 63mW
35	R12	100k	100k 5% 0402 63mW
36	R21	1k	Resistor chip, 1k 5% 0402 63mW
37	R1	220R	220R 5% 0402 63mW
38	R2	220R	220R 5% 0402 63mW
39	R4	220R	220R 5% 0402 63mW
40	R6	220R	220R 5% 0402 63mW
41	R7	220R	220R 5% 0402 63mW
42	R9	220R	220R 5% 0402 63mW
43	R18	220R	220R 5% 0402 63mW
44	R17	27k	Resistor chip, 27k 5% 0402 63mW
45	R3	4.7k	4.7k 5% 0402 63mW
46	R5	4.7k	4.7k 5% 0402 63mW
47	R10	4.7k	4.7k 5% 0402 63mW
48	R11	4.7k	4.7k 5% 0402 63mW
49	REN3	4X220R	4 x 220R ARV241
50	S1	J6_P1-P2	Jumper, Pitch, 2.54mm, Red colour
51	U1	NC7S14	Schmit-Trigger inverter
52	U3	3V0, 150mA	Reg. 3V0, 150mA
53	U5	NJG1107HB3	GaAs GAIN BLOCK NJG1107HB3

Table 7 Bill of materials

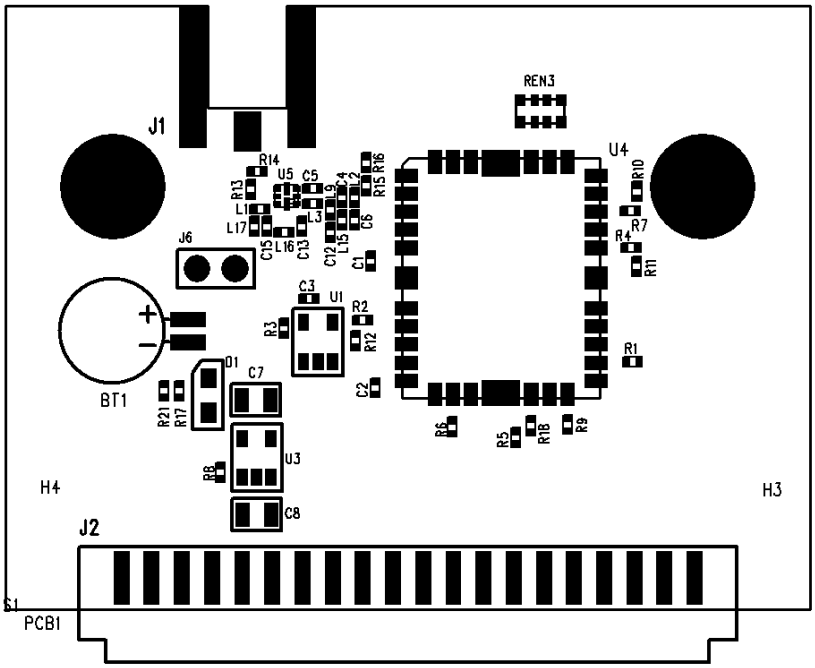
7.3 Circuit drawing

Ltr	Qty	Change	Reason / ECO no	Design	Date Review	Date Appr
B12		Module rev to IT310C06, LNA excluded				

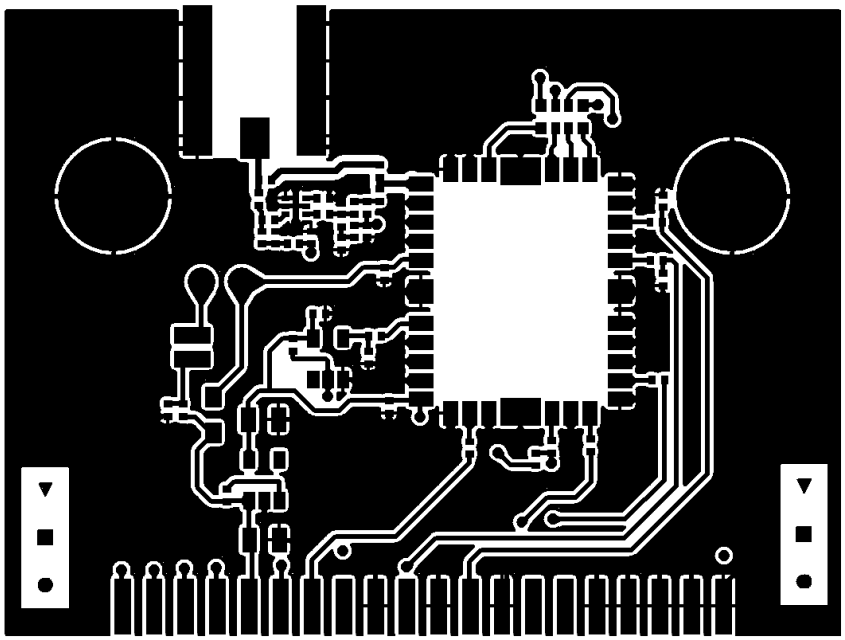


Drawn 2008-06-05	Arch Id F	Serial no	Sheet 1/1	Cooperator's doc no	
Review					
Appr					
Design KK/TS	Scale 1:1	Application Board iTRAX310		FASTRAX	
Replaces		CIRCUIT DIAGRAM		Dwg no AP310B12	Rev B
Replaced by					

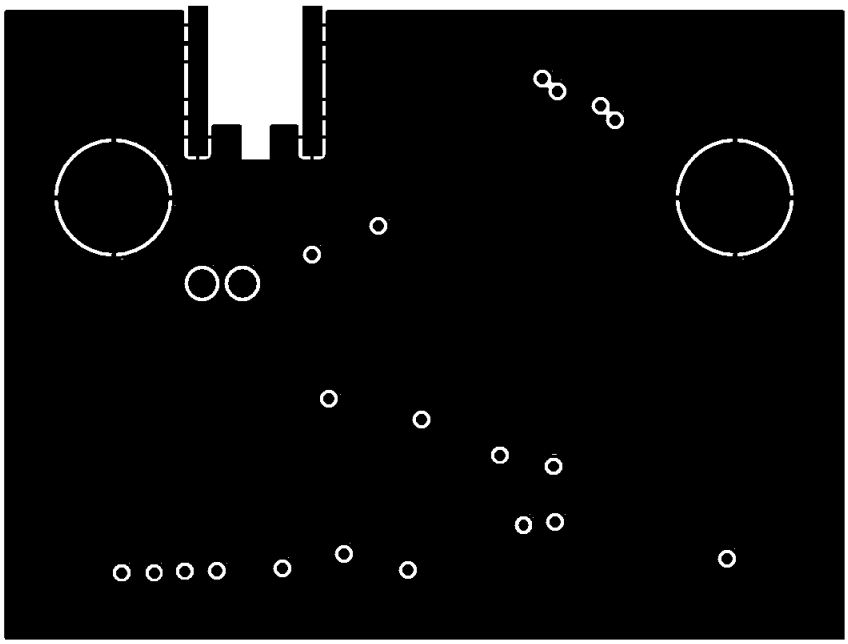
7.4 Assembly drawing, Top side



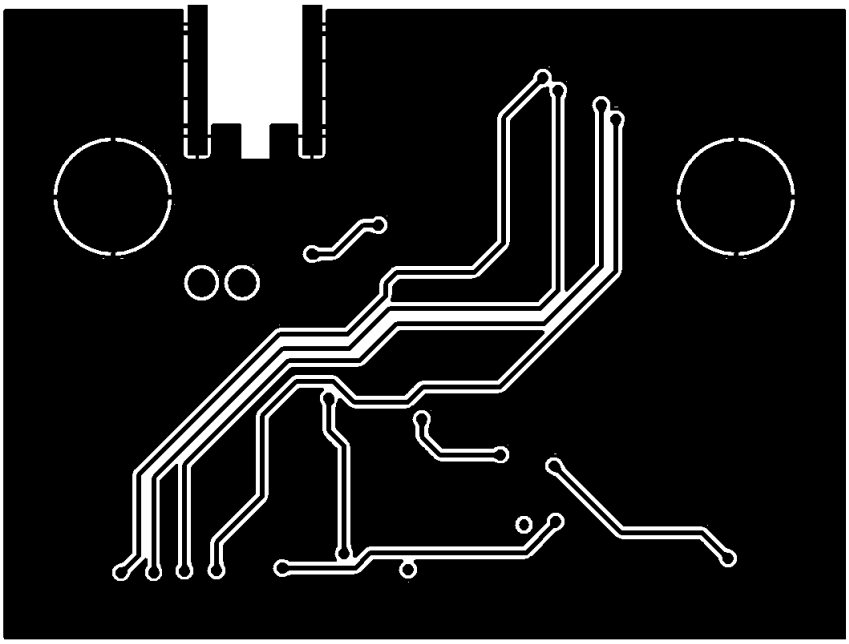
7.5 Artwork, layer 1 (Top)



7.6 Artwork, layer 2



7.7 Artwork, layer 3



7.8 Artwork, layer 4